REMARKS

The title has been amended as required by the Examiner. The specification and the drawings have been amended to correct typographical or inadvertent matters. No new matter has been added.

The Examiner's indication of allowability of claims 2-4 and 10, if rewritten in independent form, is acknowledged and appreciated. Claims 11-13 are also indicated to be allowable if rewritten to overcome the § 112, second paragraph, rejection and to include the features of the base claim and any intervenient claims.

New independent claim 19 includes features of claim 2 which the Examiner has indicated are allowable. New independent claim 20 includes features described in claim 10, which the Examiner has also indicated are allowable. Accordingly, claims 19 and 20 are believed to be in condition for allowance.

Claims 11-13 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. Claims 11-13 have been amended to now depend from claim 10, rather than claim 9. Accordingly, this rejection is now believed to have been overcome. Withdrawal of the rejection is respectfully requested.

Claims 1, 9 and 18 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Yanagi et al. Applicants respectfully traverse this rejection because the cited reference does not disclose or suggest the claimed feature for selecting a resync pattern that minimizes differences in the digital sum values (DSV) between data ranges.

The Yanagi et al. reference calculates a DSV in a data block at the time of modulating record data, and inserts a resync pattern between data blocks such that the sum of

the DSV becomes minimum, to keep the DC component of the record data constant. This method, however, results in a large fluctuation in the DC component appearing at the border between the data blocks. In systems such as a PRML system, for example, a fluctuation in the DC component at the border between data blocks degrades the capability of data reproduction.

In the present invention a resync pattern is selected that minimizes the differences in the DSV between data blocks, and inserts the selected resync pattern between the data blocks. In other words, Yanagi et al. minimizes the sum of the DSV, whereas the present invention minimizes the differences in DSV. Accordingly, Yanagi et al. neither discloses nor suggests this feature of invention as claimed. For this reason, claims 1, 9 and 18, and their respective dependent claims 2-4 and 10-13 are allowable over the cited reference.

For all of the above reasons, Applicants request reconsideration and allowance of the claimed invention. The Examiner should contact Applicants' undersigned attorney if a telephone conference would expedite prosecution.

Respectfully submitted,

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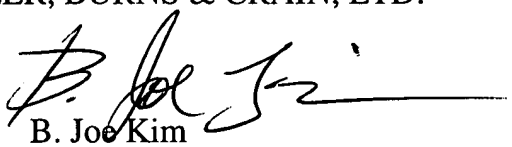
By 

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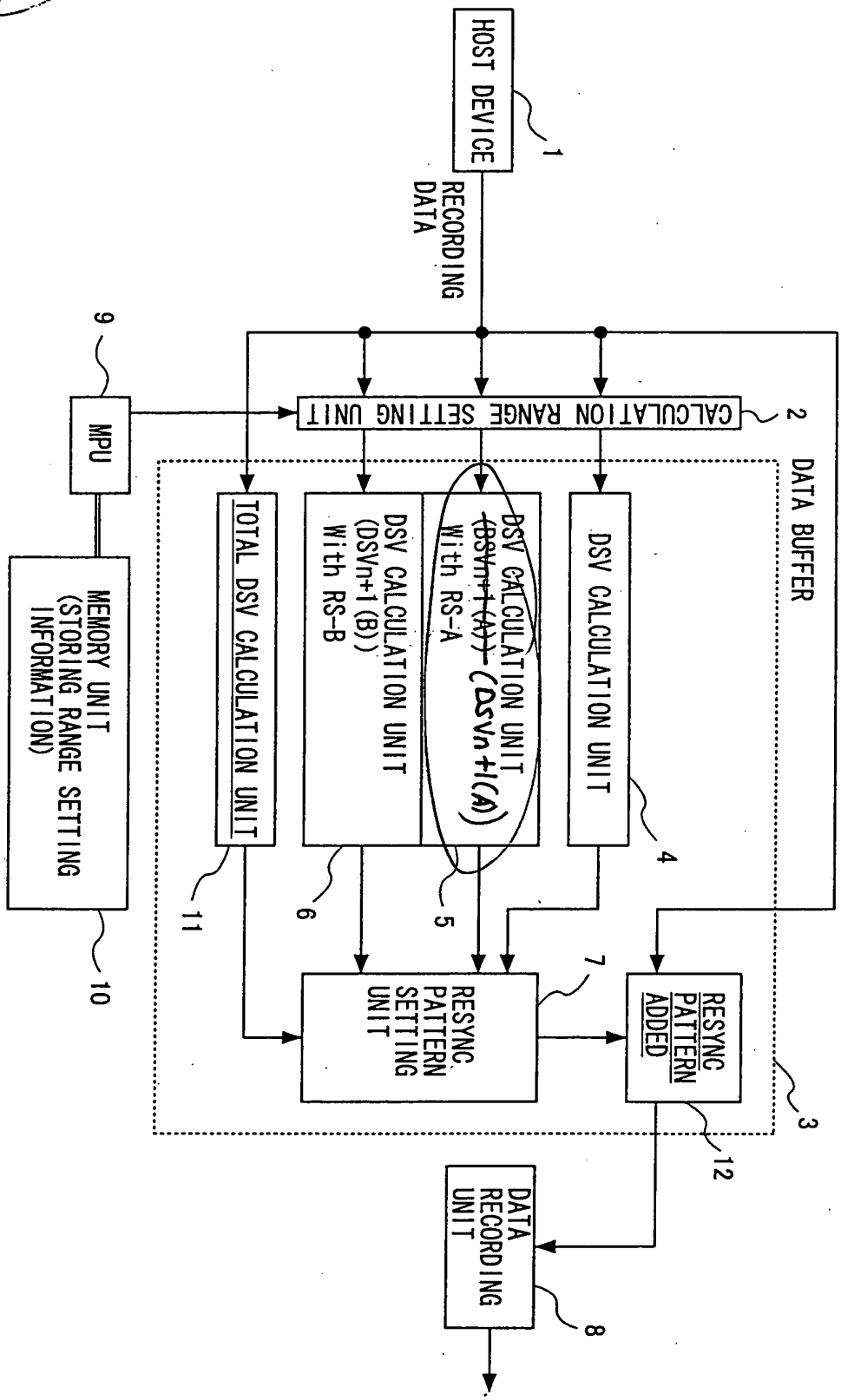

FIG.3

FIG.1